Performance Evaluation of On-chip Global Interconnects in DSM Technology using Different Signaling Techniques

Yash Agrawal[1], Rajeevan Chandel[2] and Rutu Parekh[3]
[1,3]*Member IEEE, Department of Information and Communication Technology, DA-IICT, Gandhinagar–382007, Gujarat, India*
[2]*MemberIEEE, Department of Electronics and Communication Engineering, National Institute of Technology, Hamirpur–177005, India*
E-mail: [1]mr.yashagrawal@gmail.com, [2]rchandel@nith.ac.in, [3]rutu_parekh@daiict.ac.in

***Abstract*—The research objective of the present work is to evaluate the performance of voltage and current mode signaling techniques for on-chip global interconnects. The various performance metrics are voltage swing over the interconnect line, propagation delay, power dissipation, energy, bandwidth and throughput. It is found that current mode signaling (CMS) has nearly 63% lesser delay and 162% higher bandwidth over voltage mode signaling (VMS) technique. Whereas VMS shows about 58% lesser power and energy dissipation over CMS and is thus more power and energy efficient technique for interconnects. The present work shall be useful in assessing the effectiveness of different signaling techniques for on-chip interconnect design. The results are verified using SPICE simulations for 45nm technology node.**

Keywords: Current Mode Signaling, Voltage Mode Signaling, Delay, Power Dissipation, Energy, Bandwidth, Throughput

I. INTRODUCTION

The integrated circuit (IC) technology was conceived in 1950s. Right from its advent, the prime focus has been to minimize the device size in order to embed more and more transistors on the same chip area and to achieve high functionality [1-2]. This scaling trend predicted by Moore in 1965 has continued till present day [3]. The continuous scaling of devices has pushed the dimensions of devices in nanometer range or deep submicron (DSM) technologies. Consequently, the length of long or global interconnects has increased. Thus in DSM technologies, interconnects play a vital role in determining the overall performance of the ICs.

The global on-chip interconnects that deliver clock, power and ground signals have become the governing factor in defining the VLSI system performance. The delay and power dissipation increase as the interconnect line length increases. Various techniques such as buffer insertion, use of tapered buffers have been investigated to mitigate these problems [4-5]. However, these techniques require optimum buffer sizing and spacing to achieve the best performance. Moreover, it leads to increased area overhead [6].

As an alternative to conventional buffer insertion technique, for enhanced performance of the system, various signaling techniques have been investigated for on-chip interconnects [7-14]. Current mode signaling is found to have improved performance over the conventional voltage mode signaling [11]. The current mode signaling has the advantage of reduced voltage swing over the interconnect line. This is achieved by using low impedance termination at the load. Subsequently, in the present work, voltage and current mode signaling techniques are analyzed to evaluate their performance and practical applicability for on-chip global interconnects.

The rest of the paper is organized as follows. Section II details about the voltage and current mode signaling techniques. Section III presents the model formulation for evaluation of performance parameters of interconnect. The results and comparative analysis of the two signaling schemes are also vividly discussed in the same section. Finally, conclusion is drawn in section IV.

II. VOLTAGE AND CURRENT MODE SIGNALING TECHNIQUES

The main function of interconnect is to communicate information between different modules and to provide power and ground connections. The transmission and reception of signals over interconnect are actualized by driver and receiver circuits. The driver defines the signal levels which are then transmitted through interconnects. The receiver circuit senses this signal and provides impedance matching for faithful reproduction of signals. The system consisting of driver, receiver and interconnects is shown in Fig. 1.

In voltage mode interconnect system, high impedance termination to interconnects exist. In this, interconnect is often terminated by gate of MOSFET. The MOSFET act as a receiver and possess high impedance value at its gate

 ISBN: 978-93-86724-30-4

input. As opposed to voltage mode, current mode interconnect system has small impedance termination. This is achieved by using current mode circuits. Current mode circuits have characteristics of low input and high output impedance [7-9]. Hence these provide effective low impedance termination at receiver.

The research objective of the present paper is to assess the efficacy and effect of the two prominent different on-chip signaling schemes viz. voltage and current mode in ICs. Major intentness is to assess the effectiveness between the two. For detailed comparative and first-hand comparative analysis, simplified yet considerable accurate driver, receiver and interconnect models have been preferred over strenuous elaborative models. Driver is modeled as equivalent resistive model and equivalently shown by R_D [11]. Interconnect is represented by lumped *RC* model. Receiver is equivalently modeled by R_L. The complete electrical model of interconnect system is shown in Fig. 2.

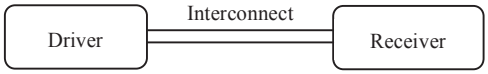


Fig. 1: An Interconnect System

The physical dimensions of interconnect are taken from ITRS [15]. The resistance and capacitance for 45nm technology node at global interconnect length of 10mm are computed as 12KΩ and 1.7pF respectively [16-17]. The driver output resistance (R_D) and receiver input resistance (R_L) for voltage mode signaling are 10kΩ and 10MΩ respectively. Similarly, for current mode signaling, values of R_D and R_L are 40kΩ and 10kΩ respectively. These values are computed from the driver and receiver circuits proposed in [14].

III. Modeling and Analysis the Performance Parameters of Interconnect System

In this section, analytical model for evaluating the performance parameters of interconnect system for both voltage and current mode signaling techniques has been systematically presented. The performance metrics considered are (i) voltage swing over interconnect, (ii) propagation delay, (iii) power dissipation, (iv) energy dissipation and (v) bandwidth. The analytical results are validated using SPICE simulations [18].

A. Voltage Swing Over Interconnect

Voltage swing defines the signal level over interconnects. For the analysis, square input signal has been considered as shown in Fig. 3 [19-20]. During charging period (T_1) of input signal, the branch currents flowing through different elements of the equivalent circuit of Fig. 2 are shown in Fig. 4.

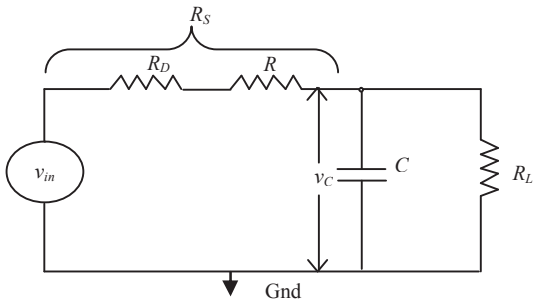


Fig. 2: Electrical Equivalent Model of Interconnect

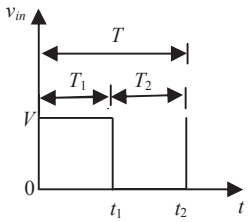


Fig. 3: Input Square Wave Signal

Applying Kirchhoff's current law (KCL) at node A in Fig. 4, gives

$$i_{R_S\_T_1} = i_{C\_T_1} + i_{R_L\_T_1} \tag{1}$$

This can be written as

$$i_{R_S\_T_1} = C\frac{dv_{C\_T_1}}{dt} + \frac{v_{C\_T_1}}{R_L} \tag{2}$$

where $i_{R_S\_T_1}$, $i_{R_L\_T_1}$ and $i_{C\_T_1}$ are current through R_S, R_L and C respectively during charging period (T_1). $v_{C\_T_1}$ and V are voltage across capacitor and input voltage during charging period.

Applying Kirchhoff's voltage law (KVL) in input loop, leads to

$$V = i_{R_S\_T_1}R_S + v_{C\_T_1} \tag{3}$$

Substituting (2) in (3), gives

$$V = \left(C\frac{dv_{C\_T_1}}{dt} + \frac{v_{C\_T_1}}{R_L}\right)R_S + v_{C\_T_1} \tag{4}$$

This can be written as

$$\frac{dv_{C\_T_1}}{dt} + \frac{(R_S + R_L)}{R_S R_L C}v_{C\_T_1} = \frac{V}{R_S C} \tag{5}$$

Eq. (5) is first order differential equation, with solution as

$$v_{C\_T_1} = v_{CH\_T_1} + v_{CP\_T_1} \tag{6}$$

where, $v_{CH\_T_1}$ is a homogeneous solution and $v_{CP\_T_1}$ is a particular solution of the differential equation during charging period.

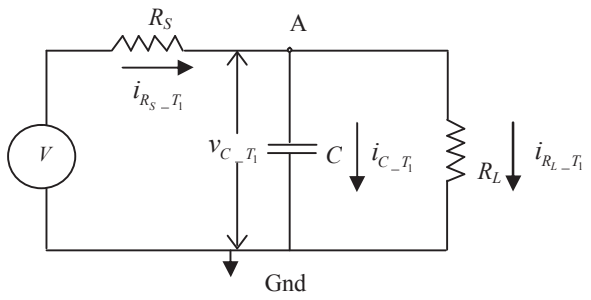


Fig. 4: Equivalent Circuit During Charging Period (T_1)

The homogeneous solution is computed as

$$v_{CH\_T_1} = \frac{dv_{C\_T_1}}{dt} + \frac{v_{C\_T_1}}{R_{eq}C} = 0 \tag{7}$$

where,

$$R_{eq} = \frac{R_S R_L}{R_S + R_L} \tag{8}$$

Solving this we get,

$$v_{CH\_T_1} = Ke^{-t/R_{eq}C} \tag{9}$$

The particular solution is computed as

$$v_{CP\_T_1} = \frac{1}{\left(D + \frac{1}{R_{eq}C}\right)} \frac{V}{R_S C} \tag{10}$$

where,

$$D = \frac{d}{dt} \tag{11}$$

It gives the value of $v_{CP\_T_1}$ as

$$v_{CP\_T_1} = \frac{R_{eq}}{R_S} V \tag{12}$$

From eqs. (7), (9) and (12), the solution obtained is

$$v_{C\_T_1} = Ke^{-t/R_{eq}C} + \frac{R_{eq}}{R_S} V \tag{13}$$

Using boundary condition, that at $t = 0$, $v_{C\_T_1} = 0$

The voltage obtained across the capacitor during charging period is

$$v_{C\_T_1} = \frac{R_{eq}}{R_S}\left(1 - e^{-t/R_{eq}C}\right).V \tag{14}$$

Voltage swing is the difference between the maximum and the minimum output voltages. By substituting $t = \infty$ in (14), the maximum output voltage is obtained. The minimum output voltage is zero for input square wave signal (shown in Fig. 3). The analytical and simulation results for voltage swing are presented in Table 1.

The input and output waveforms are shown in Fig. 5. It can be seen from the figure that current mode signaling has reduced output voltage swing as compared to that in voltage mode signaling technique. However, the output voltage in current signaling mode is less distorted and maintains good signal integrity. This results in lesser delay and higher throughput.

TABLE 1: UNITS FOR MAGNETIC PROPERTIES VOLTAGE SWING FOR VOLTAGE AND CURRENT MODE SIGNALING TECHNIQUES FOR INTERCONNECT SYSTEM

Signaling Type	Voltage Swing (in Volts)	
	SPICE	Analytical
Voltage mode	0.99 V	0.997V
Current mode	161 mV	161 mV

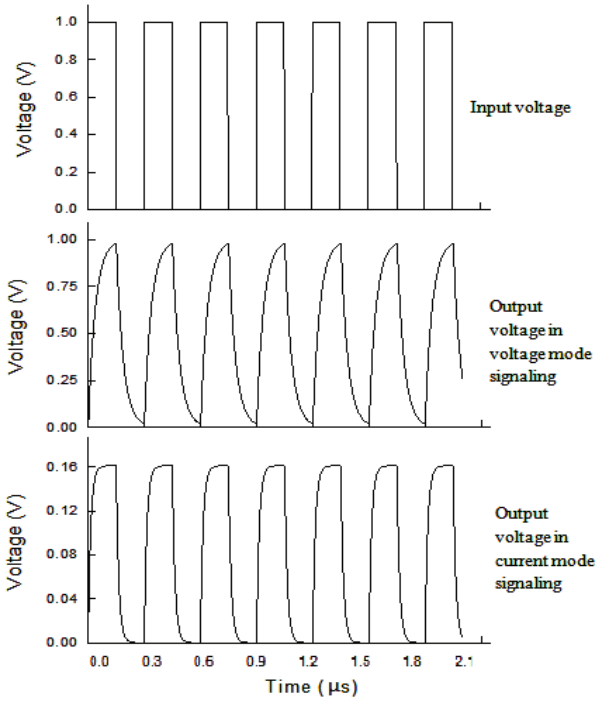


Fig. 5: Waveform Showing Voltage Swing for Voltage and Current Mode Signaling Scheme

B. *Propagation Delay*

Propagation delay is one of the effective performance parameters to access the system efficiency in terms of speed. It depicts the transient behavior of the circuit. A system with lesser delay has faster operation. Here for analysis, 50% delay is computed. The 50% delay is defined as the time difference output voltage takes to reach 50% of its maximum value with respect to 50% value of the input voltage. Further, the analytical model for propagation delay is developed.

Eq. (14) gives the capacitor output voltage of the circuit shown in Fig. 4. If t is very large, then from (14) maximum output voltage can be approximated as

$$v_{C\_T_1 \max} \approx \frac{R_{eq}}{R_S} V \tag{15}$$

Using (14) and (15), time taken for output voltage to reach 50% of its maximum value is computed as

$$0.5v_{C\_T_1 \max} = 0.5\frac{R_{eq}}{R_S}V = \frac{R_{eq}}{R_S}\left(1-e^{-t_{o/p\_50\%}/R_{eq}C}\right).V \tag{16}$$

Solving this we get,

$$t_{o/p\_50\%} = -R_{eq}C.\ln(0.5) \tag{17}$$

Assuming input rise time as 1ns, then time required by input voltage to reach 50% of its maximum value is:

$$t_{i/p\_50\%} = 0.5ns \tag{18}$$

Hence, 50% delay is computed as

$$t_{50\%} = t_{o/p\_50\%} - t_{i/p\_50\%} \tag{19}$$

The fifty percent delay for voltage and current mode signaling using SPICE simulations and analytical computation is given in Table 2.

TABLE 2: 50% DELAY FOR VOLTAGE AND CURRENT MODE SIGNALING SCHEMES FOR INTERCONNECT SYSTEM

Signaling Type	Delay (ns)		% Error
	SPICE	Analytical	
Voltage mode	25.77	25.36	1.616%
Current mode	9.854	9.37	5.165%

From Table 2, it can be inferred that delay in current mode signaling is lesser as compared to voltage mode signaling technique. From analytical model, it is observed that CMS has 63.05% lesser delay than VMS.

This is so because current mode signaling technique has reduced voltage swing over the interconnect line. This enables fast charging and discharging of interconnect parasitic capacitances. The small delay in current mode signaling results in faster operation of the system.

C. *Power Dissipation and Energy*

Power dissipation and energy are important parameters for low power applications. These parameters define the battery life-time of portable gadgets and the amount of heat generated in circuit. Higher power dissipation results in higher energy consumption rate and consequently leads to faster exhaustion of battery. Moreover, this in turn generates more heat. To dissipate this heat, heat sinks are required. These are the system overheads and make system bulky [21].

The total instantaneous power dissipation can be obtained by summing together the total instantaneous power dissipation during charging period (T_1) and discharging period (T_2). This is formulated as

$$P_{inst\_total}(t) = P_{inst\_T_1}(t) + P_{inst\_T_2}(t) \tag{20}$$

During charging period (T_1), the equivalent circuit is same as Fig. 4. The instantaneous power dissipation is derived as:

$$P_{inst\_T_1}(t) = \frac{\left(V - v_{C\_T_1}\right)^2}{R_s} + \frac{\left(v_{C\_T_1}\right)^2}{R_L} \tag{21}$$

where,

$$v_{C\_T_1} = \left(\frac{R_L}{R_S + R_L}\right)\left(1-e^{-t/R_{eq}C}\right)\cdot V \tag{22}$$

During discharging period (T_2), the equivalent circuit is as shown in Fig. 6.

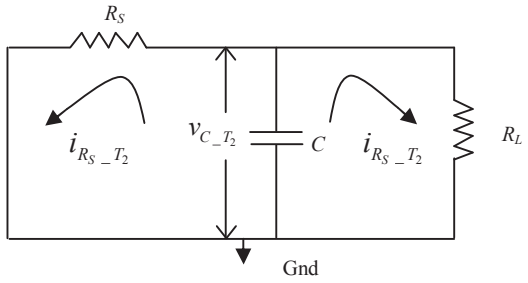


Fig. 6: Equivalent Circuit During Discharging Period (T_2)

The instantaneous power dissipation during discharging period T_2 is formulated as

$$P_{inst\_T_2}(t) = \frac{{v_{C\_T_2}}^2}{R_S} + \frac{{v_{C\_T_2}}^2}{R_L} \tag{23}$$

where, $v_{C\_T_2}$ is the voltage across capacitor and is given as

$$v_{C\_T_2} = \left(\frac{R_L}{R_S + R_L}\right)\left(e^{-(t-t_1)/R_{eq}C}\right)\cdot V \tag{24}$$

Now energy dissipation is computed by integrating instantaneous power dissipation over a period of time. The energy dissipation during charging period (T_1) is given as

$$E_{T_1}(t) = \int_0^{t_1} P_{inst\_T_1}\, dt \tag{25}$$

Using eqs. (21) and (25), gives

$$E_{T_1}(t) = \int_0^{t_1}\left(\frac{\left(V - v_{C\_T_1}\right)^2}{R_S} + \frac{\left(v_{C\_T_1}\right)^2}{R_L}\right)dt \tag{26}$$

Solving this leads to

$$E_{T_1} = \frac{V^2}{\left(R_S + R_L\right)}T_1 + \frac{C}{2}\left(\frac{R_L}{R_s + R_L}V\right)^2\left(1-e^{-T/R_{eq}C}\right) \tag{27}$$

Similarly during discharging period (T_2), energy dissipation is given as

$$E_{T_2}(t) = \int_{t_1}^{t_2} P_{inst\_T_2}\, dt \tag{28}$$

Using eqs. (23) and (28)

$$E_{T_2}(t) = \int_{t_1}^{t_2}\left(\frac{{v_{C\_T_2}}^2}{R_S} + \frac{{v_{C\_T_2}}^2}{R_L}\right)dt \tag{29}$$

Solving this, we get

$$E_{T_2} = \frac{C}{2}\left(\frac{R_L}{R_S + R_L}V\right)^2\left(1-e^{-T/R_{eq}C}\right) \tag{30}$$

The total energy dissipation is the sum of energy dissipation during charging and discharging period and is given as

$$E_{total} = E_{T_1} + E_{T_2} \tag{31}$$

Using equations (27), (30) and (31),

$$E_{total} = \frac{V^2}{(R_S + R_L)} T_1 + \left[\frac{C}{2} \left(\frac{R_L}{R_S + R_L} V \right)^2 \left(2 - 2e^{-T/R_{eq}C} \right) \right] \tag{32}$$

Using (32), energy dissipation for voltage and current mode signaling is computed and presented in Table 3. It is seen from the Table that voltage mode signaling has 57.8% lesser energy dissipation than current mode signaling technique.

The average power dissipation is defined as the energy consumption rate and is given as

TABLE 3: ENERGY DISSIPATION FOR INTERCONNECT SYSTEMS

Signaling Type	Energy (pJ)		% Error
	SPICE	Analytical	
Voltage mode	1.69	1.71	1.16%
Current mode	4.06	4.07	0.24%

$$P_{avg} = \frac{E_{total}}{T} \tag{33}$$

Using eqs. (32) and (33)

$$P_{avg} = \frac{V^2}{(R_S + R_L)} \frac{T_1}{T} + \left[\frac{C}{2T} \left(\frac{R_L}{R_S + R_L} V \right)^2 \left(2 - 2e^{-T/R_{eq}C} \right) \right] \tag{34}$$

For symmetrical square wave, $T_1 = T_2 = T/2$

$$P_{avg} = \frac{V^2}{2(R_S + R_L)} + \left[\frac{C}{2T} \left(\frac{R_L}{R_S + R_L} V \right)^2 \left(2 - 2e^{-T/R_{eq}C} \right) \right] \tag{35}$$

The first term is independent of time period and it gives the static power dissipation (P_{static}) whereas the second term is a related to charging and discharging of capacitor and depends on time period of square wave and it gives the dynamic power dissipation ($P_{dynamic}$).

Hence,

$$P_{static} = \frac{1}{2} \left(\frac{v_{in}^2}{R_S + R_L} \right) \tag{36}$$

$$P_{dynamic} = \frac{1}{2} \frac{C}{T} \left(\frac{R_L}{R_S + R_L} V \right)^2 \left(2 - 2e^{-T/R_{eq}C} \right) \tag{37}$$

The average power dissipation for voltage and current mode signaling is computed using (35). The SPICE and analytical variations for voltage and current mode are 1.107% and 0.22% respectively as seen in Table IV. It can be seen from the Table that in voltage mode signaling, static power dissipation constitutes merely 1.45% while dynamic power dissipation dominantly constitutes 98.55%. However, in current mode signaling, static power dissipation constitutes the major portion of total power dissipation and it comes to 98.92% while dynamic power dissipation is only 1.08%. The dynamic power is reduced in current mode signaling. It is due to the reduced voltage swing over the interconnect line. The static power is increased due to increased current signal over the interconnect line. The percentage distribution of average power dissipation in voltage and current mode signaling techniques are shown in Figs. 7(a) and (b) respectively. From Figs. 7(a) and (b), it can be analyzed that in current mode signaling, static power dissipation is much higher as compared to voltage mode signaling technique. For low power applications, this power dissipation must be minimized. This can be accomplished by using various encoding schemes and circuit techniques [22-25]. In [22], a standard power gated current mode logic cell library featuring a sleep transistor in every cell is proposed. In [23], pulse dual rail encoding is used. Selective signal gating is proposed to minimize power dissipation in [24]. These techniques can be used in current mode signaling interconnects to minimize energy and static power dissipation. It is seen from Table 4 that the analytical and SPICE results show a good agreement.

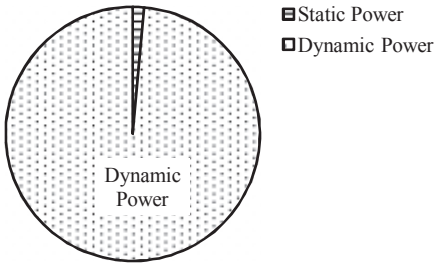
TABLE 4: AVERAGE POWER DISSIPATION FOR VOLTAGE AND CURRENT MODE SIGNALING SCHEMES FIR INTERCONNECT SYSTEM

Signaling Type	SPICE	Analytical			%Error
	P_{total} (µW)	P_{static} (uW)	$P_{dynamic}$ (uW)	P_{total} (uW)	
Voltage mode	3.392	0.0499	3.38	3.43	1.107%
Current mode	8.13	8.06	0.0884	8.148	0.22%

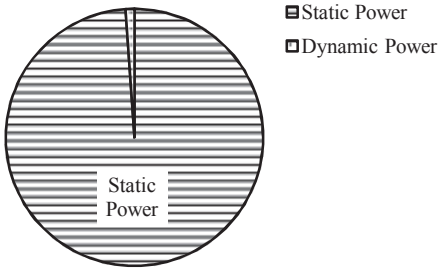
D. *Bandwidth*

Bandwidth is defined as the range of frequencies for transmission of signal. The maximum allowable frequency gives the higher cutoff frequency. Thevenin's equivalent circuit model for interconnect system (Fig. 4) is shown in Fig. 8 and is used to analyze bandwidth in the signaling techniques.

In Fig. 8, v_{Th} *and* R_{eq} are Thevenin equivalent voltage and resistance respectively.



(a) Voltage mode signaling (VMS)



(b) Current mode signaling (CMS)

Fig. 7: Percentage Distribution of Power Dissipation in (a) VMS and (b) CMS

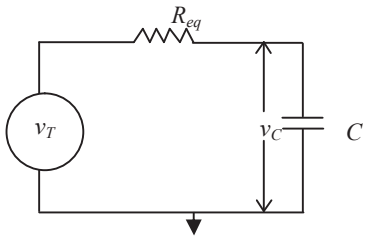


Fig. 8: Thevenin's Equivalent Model

The transfer function *H(w)* is

$$H(w) = \frac{v_C}{v_{Th}} = \frac{1/jwC}{R_{eq} + 1/jwC} \tag{38}$$

where, *w* is angular frequency.

Substituting w=2πf, transfer function becomes

$$H(2\pi f) = \frac{1}{1 + j2\pi f R_{eq} C} \tag{39}$$

It can be written as

$$H(2\pi f) = \frac{1}{1 + j\,f/f_{CH}} \tag{40}$$

where

$$f_{CH} = \frac{1}{2\pi R_{eq} C} \tag{41}$$

From eq. (41), higher cutoff frequency for voltage and current mode signaling is computed. Assuming lower cutoff frequency as zero. The bandwidth is computed as the difference between higher and lower cutoff frequencies.

AC analysis computes bandwidth using SPICE simulation. Frequency at 3dB of maximum output voltage gives the higher cutoff frequency. Analytically bandwidth is computed using eq. (42).

$$Bandwidth = f_{CH} - f_{CL} \tag{42}$$

The simulated and analytical results obtained for bandwidth computation for interconnect system are tabulated in Table V. A good agreement is seen between analytical and SPICE results. From the Table, it is observed that for analytical model, current mode signaling has 6.905MHZ higher bandwidth as compared to voltage mode signaling technique. Thus, CMS has 2.61 times higher bandwidth than VMS technique.

TABLE 5: BANDWIDTH FOR VOLTAGE AND CURRENT MODE SIGNALING SCHEMES FOR INTERCONNECT SYSTEM

Signaling Type	Bandwidth (MHz)		% Error
	SPICE	Analytical	
Voltage mode	4.264	4.265	0.02%
Current mode	11.21	11.17	0.35%

IV. CONCLUSION

In the present work voltage and current mode signaling for on-chip VLSI interconnects has been analyzed. It is seen that current mode signaling has lesser delay, higher bandwidth and smaller voltage swing as compared to voltage mode signaling. However, static power dissipation and energy dissipation are higher in current mode signaling. These can be minimized in current mode signaling scheme by incorporating proper encoding schemes and by special circuit design techniques. Consequently, from the present work it is inferred that current mode signaling technique is beneficial for VLSI applications requiring lower latency and higher bandwidth while voltage mode signaling is good for power and energy efficient systems.

REFERENCES

[1] C. Phipps, "The Early History of ICs at Texas Instruments: A Personal View," *IEEE Annals of the History of Computing*, vol. 34, no. 1, pp. 37-47, Jan. 2012.

[2] J. S. Kilby, "The Integrated Circuit's Early History," *Proc. IEEE*, vol. 88, no. 1, pp. 109-111, Jan. 2000.

[3] C. A. Mack, "Fifty Years of Moore's Law," *IEEE Trans. on Semiconductor Manufacturing*, vol. 24, no. 2, pp. 202-207, 2011.

[4] R. Chandel, S. Sarkar, and R. P. Agarwal, "An Analysis of Interconnect Delay Minimization by Low-Voltage Repeater Insertion," *Microelectronics J., Elsevier Science*, vol. 38, no. 45, pp. 649-655, April-May 2007.

[5] K. Banerjee and A. Mehrotra, "A Power-Optimal Repeater Insertion Methodology for Global Interconnects in Nanometer Designs," *IEEE Trans. on Electron Devices*, vol. 49, no. 11, pp. 2001-2007, Nov. 2002.

[6] H. Zhou, D. F. Wong, I. M. Liu and A. Aziz, "Simultaneous Routing and Buffer Insertion with Restrictions on Buffer Locations," *IEEE Trans. on Computer Aided Design of Integrated Circuits and Systems*, vol. 19, no. 7, pp. 819824, July 2000.

[7] Y. Agrawal, M. G. Kumar, and R. Chandel, "Comprehensive model for high-speed current-mode signaling in next generation MWCNT bundle interconnect using FDTD technique," *IEEE Trans. Nanotechnol.*, vol. 15, no. 4, pp. 590–598, Jul. 2016.
[8] N. Tzartzanis and W. W. Walker, "Differential Current-Mode Sensing for Efficient On-Chip Global Signaling," *IEEE J. of Solid-State Circuits*, vol. 40, no. 11, pp. 2141-2147, Nov. 2005.
[9] T. Wang and F. Yuan, "A New Current-Mode Incremental Signaling Scheme with Applications to Gb/s Parallel Links," *IEEE Trans. on Circuits and Systems,* vol. 54, no. 2, pp. 255-267, Feb. 2007.
[10] S. Joshi and D. Sharma, "A Novel Low Power Multilevel Current Mode Interconnect System," *IEEE Proc. of the Emerging VLSI Technologies and Architectures*, pp. 1-6, 2006.
[11] R. Bashirullah, W. Liu and R. K. Cavin, "Current-Mode Signaling in Deep Submicrometer Global Interconnects," *IEEE Trans. on Very Large Scale Integration Systems*, vol. 11, no. 3, pp. 406-417, Jan. 2003.
[12] Y. Agrawal, M. G. Kumar, R. Chandel, "A novel unified model for copper and MLGNR Interconnects using voltage- and current-mode signaling schemes," *IEEE Trans. Electromagn. Compat.*, vol. 59, pp. 217–227, 2016.
[13] A. Narasimhan, M. Kasotiya and R. Sridha, "A Low-Swing Differential Signaling Scheme for On-chip Global Interconnects," *IEEE 18th Int. Conf. on VLSI Design*, pp. 634-639, 2005.
[14] Y. Agrawal, R. Chandel, and R. Dhiman, "High performance current mode receiver design for on-chip VLSI interconnects," chapter 54, *Springer Proc. Int. Conf. ICA. Series: Advances in Intelligent Systems and Computing*, vol. 343, pp. 527-536, Feb. 2015.
[15] International Technology Roadmap for Semiconductors (ITRS), 2014. Available at: http://public.itrs.net.
[16] S. C. Wong, G. Y. Lee and D. J. Ma, "Modeling of Interconnect Capacitance, Delay and Crosstalk in VLSI," *IEEE Trans. on Semiconductor Manufacturing*, vol. 13, no. 1, pp. 108-111, Feb. 2002.
[17] Predictive Technology Models, 2014. Available at: http://www.ptm.asu.edu.
[18] Tanner EDA tools, 2014. Available at: http://www.tanner.com.
[19] A. Agarwal and J. H. Lang, *Foundation of Analog and Digital Electronic Circuits*, Elsevier, 2005.
[20] W. J. Dally and J. W. Poulton, *Digitals Systems Engineering*, Cambridge University, 2011.
[21] Fei Yuan, *CMOS Current Mode Circuits for Data Communication*, Springer, 2007.
[22] A. Cevrero, et. al, "Power-Gated MOS Current Mode Logic (PG-MCML): a Power Aware DPA-Resistant Standard Cell Library," *IEEE 48th Design Automation Conf. DAC*, pp. 1014-1019, June 2011.
[23] E. Nigussie, J. Plosila and Jouni Isoaho, "Semi-Serial On-Chip Link Implementation for Energy Efficiency and High Throughput," *IEEE Int. Symp. on Circuits and Systems ISCAS*, pp. 649-652, 2007.
[24] M. S. Bhat and H. S. Jamadagni, "Static Power Minimization in Current-Mode Circuits," *IEEE Proc. of the Design Automation Conference DAC*, pp. 1220-1223, 2005.

BIOGRAPHIES

Yash Agrawal received B.E. Degree in Electronics and Communication Engineering from Kavikulguru Institute of Technology, Ramtek, Maharashtra, India, in 2009 and M.Tech. and Ph.D. Degrees in VLSI Design Automation and Techniques from National Institute of Technology, Hamirpur, Himachal Pradesh, India, in 2012 and 2016, respectively. Presently, he is working as Assistant Professor at DA-IICT Gandhinagar, Gujarat. His current research interests include design techniques and modelling of high-speed on-chip VLSI interconnects, numerical techniques.

He achieved university rank during his Bachelor's degree. He achieved the third place in All India Mentor Graphics design contest held at Bangalore, India in 2011. He has been the chairman and awarded with best forum member of IETE Students' Forum at KITS Ramtek, Nagpur Division during 2008–2009. He has also been awarded first rank in various national and inter-college level paper presentations.

Rajeevan Chandel received B.E. degree in Electronics and Communication Engineering from Thapar University Patiala, India, in 1990. She is a double gold medalist of Himachal Pradesh University, Shimla, India, in Pre-University and Pre-Engineering in 1985 and 1986, respectively. She received M.Tech. degree in Integrated Electronics and Circuits from Indian Institute of Technology (IIT), Delhi, India, in 1997. She was awarded Ph.D. degree from IIT Roorkee, India, under QIP scheme of Govt. of India in 2005. Dr Chandel joined the Department of Electronics and Communication Engineering,

NIT Hamirpur, HP India, as a lecturer in 1990, where presently she is working as a professor and has been the Head of the department twice. She has five MHRD, MCIT sponsored projects to her credit from the Govt. of India. She has over 50 research papers in international and national journals of repute and over 75 in conferences. Her research interest includes electronics circuit modelling and low-power VLSI design. She is a Fellow of IETE(I), Member of IEEE and Life Member of ISTE(I) and ISSS.

Rutu Parekh received her M. Eng. in Electrical Engineering from Concordia University, Canada, PhD in Electrical Engineering (Nanoelectronics) from Université de Sherbrooke, Canada and Postdoctoral fellow at Centre of Excellence in Nanoelectronics, IIT Bombay in 2015. She is currently working as a Faculty at DA-IICT, India. Her research interest includes developing models, co-design methodology and co-simulation of hybrid circuits of emerging nanoelectronic devices with CMOS technology, low voltage low power circuits, embedded systems and IOE.